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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known

Application Number	Not yet assigned
Filing Date	June 28, 2001
First Named Inventor	Keeth et al.
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	DB000575-014

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.†	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number	Kind Code‡ (if known)			class	sub
AS		6,043,118		Suwanai et al.	03/28/2000	438	253
		5,960,455		Bauman	09/28/1999	711	120
		5,838,627		Tomishima et al.	11/17/1998	365	230.03
		5,677,645		Merritt	10/14/1997	327	536
		5,651,011		Keeth	07/22/1997	714	724
		5,614,859		Ong	03/25/1997	327	333
AS		5,574,697		Manning	11/12/1996	365	226
		5,557,579		Raad et al.	09/17/1996	365	226
		5,552,739		Keeth et al.	09/03/1996	327	538
		5,526,364		Roohparvar	06/11/1996	714	724
		5,519,360		Keeth	05/21/1996	331	57
AS		5,481,179		Keeth	01/02/1996	323	315
		5,379,263		Ogawa et al.	01/03/1995	365	230.04
		5,373,227		Keeth	12/13/1994	323	313
		5,266,821		Chern et al.	11/30/1993	257	312
		5,231,605		Lee	07/27/1993	365	201
AS		5,212,440		Waller	05/18/1993	323	313
		5,159,273		Wright et al.	10/27/1992	324	537
		5,155,704		Walther et al.	10/13/1992	365	201
AS		4,970,725		McEnroe et al.	11/13/1990	714	25

FOREIGN PATENT DOCUMENTS

[illegible]

**Examiner
Signature**

Dr. Tran

Date Considered

7/28/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO			Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	Not yet assigned
			Filing Date	June 28, 2001
			First Named Inventor	Keeth et al.
			Group Art Unit	Not yet assigned
			Examiner Name	Not yet assigned
			Attorney Docket Number	DB000575-014
Sheet	2	of	3	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
AT		SUGIBAYASHI ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		TAGUCHI ET AL., "A 40-ns 64-Mb DRAM with 64-b Parallel Data Bus Architecture", IEEE Journal of Solid-State Circuits, Vol. 26 (No. 11), (November 1991)	
		KITSUKAWA ET AL., "256-Mb DRAM Circuit Technologies for File Applications", IEEE Journal of Solid-State Circuits, Vol. 28 (No. 11), (November 1993)	
		JEDEC SOLID STATE PRODUCTS ENGINEERING COUNCIL, "Committee Letter Ballot", JC-42.3-95-73, Item #633.13, Arlington, VA (April 1995)	
AS		YOO ET AL., "SP 23.6: A 32-Bank 1Gb DRAM with 1 GB/s Bandwidth", ISSCC96/Session 23/DRAM/PAPER SP 23.6	
		NITTA ET AL., "SP 23.5: A 1.6GB/s Data-Rate 1Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", ISSCC96/Session 23/DRAM PAPER SP 23.5	
		U.S. Patent Application S.N. 08/521,563, entitled IMPROVED VOLTAGE REGULATOR CIRCUIT, filed 8/30/95	
		U.S. Patent Application S.N. 08/668,347, entitled DIFFERENTIAL VOLTAGE REGULATOR, filed 6/26/96	
MT		U.S. Patent Application S.N. 08/460,234, entitled SINGLE DEPOSITION LAYER METAL DYNAMIC RANDOM ACCESS MEMORY, filed 8/17/95	
		U.S. Patent Application S.N. 08/420,943, entitled DYNAMIC RANDOM-ACCESS MEMORY, filed 6/4/95	
AT		U.S. Patent Application S.N. 08/194,184, entitled INTEGRATED CIRCUIT POWER SUPPLY HAVING PIECEWISE LINEARITY, filed 2/8/94	

Examiner Signature	M. TRAN	Date Considered	7/28/04
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Sheet	3	of	3		

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Examiner Signature	M. TRAN	Date Considered	7/28/04
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